In Re: James R. Eaton, Jr. et al.

Serial No. 10/661,448

Attorney Doc. No.: 5649-2248

Page 2 of 5

Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims of this application:

Listing of Claims:

- 1-6. (Canceled).
- 7. (Currently amended) The MRAM according to Claim 6 A Magnetic Random Access Memory (MRAM) device comprising:

an array of magnetic memory cells arranged in intersecting rows and columns;

a plurality of magnetic memory cell selection devices, each of which is coupled to a respective one of the magnetic memory cells in the array to enable selective access to any of the magnetic memory cells during a write operation, wherein the a number of the rows and eolumns included in the device array is limited according to the relation:

$$\eta = \sqrt{\frac{R_m * \varepsilon (2 + K_{DR})}{R_r (1 - \varepsilon)}}$$

where R_m comprises a resistance of one of the magnetic memory cells, ε comprises a maximum current non-uniformity of the array during a write operation, K_{DR} depends on the a reverse bias resistance of one of the magnetic memory cell selection devices, and R_r comprises a resistance of a row or column of the magnetic memory cells.

- 8. (Previously presented) The MRAM according to Claim 7 wherein the maximum current non-uniformity of the array comprises less than about 15 percent.
 - 9. (Canceled).

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Page 3 of 5

10. (Currently amended) The MRAM according to Claim [[6]] 7 wherein the magnetic memory cell selection devices comprises diodes or transistors.

- 11. (Canceled).
- 12. (Currently amended) The method according to Claim 11 A method of sizing a MRAM comprising:

determining a maximum current non-uniformity for the MRAM array to be provided by the array during a write operation wherein the maximum number of rows and columns for inclusion in the device is limited according to the relation:

$$\eta = \sqrt{\frac{R_m * \varepsilon (2 + K_{DR})}{R_r (1 - \varepsilon)}}$$

where R_m comprises a <u>cell</u> resistance of one of the magnetic memory cells, ε comprises a maximum current non-uniformity of the array during a write operation, K_{DR} depends on the reverse bias resistance of one of the magnetic memory cell selection devices, and R_r comprises a resistance of a row or column of the magnetic memory cells

- 13. (Previously presented) The method according to Claim 12 wherein the maximum current non-uniformity of the array comprises less than about 15 percent.
 - 14. (Canceled).
- 15. (Currently amended) The method according to Claim [[11]] 12 wherein the magnetic memory cell selection devices comprises diodes or transistors.
 - 16. (Canceled).